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EXAMINER

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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 09/985,763
Filing Date: November 06, 2001
Appellant(s): KALAPATHY ET AL.

MAILED

MAR - 9 2007

GROUP 2600

Paul Kalapathy et al
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 12/19/2006 appealing from the office action mailed 8/23/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6453358

Michels

9-2000

Kalapathy, Paul, "The specification of the pending application", paragraph [0055]; lines 1-7

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 2, 4, 6-8, 10, 12, 13, 15-17, 19 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Michels et al (U.S. 6453358), hereinafter referred to as Michels.

Re claims 1, 7, 13, and 16, Michels discloses a search device including a primary memory (*a table of claims 1 and 13, a table means of claim 7, an address resolution (ARL) table of claim 16, figure 3, element 58*) with a lookup table (*having a plurality of entries, column 5, lines 39-40*), a stage 1 memory (*a cache of claims 1 and 13, a cache means of claim 7, an ARL cache table of claim 16, figure 3, element 70*) that does not contain the entire lookup table (*having a subset of entries of said plurality of entries of the table, column 6, lines 5-10*), and two binary search engines (*a search engine of claim 1 and 16, a search engine means of claim 7, figure 3, elements 66 and 68*). Two binary search engines (figure 3, elements 66 and 68) constitute a search engine. Michels discloses the first binary search engine (figure 3, element 66) connected to a stage 1

memory (figure 3, element 70) and the second binary search engine (figure 3, element 68) connected to a primary memory (figure 3, element 58) (*a search engine is connected to the table of claim 1, the ARL table of claim 16 and the cache of claim 1 or the ARL cache table as in claim 16*). The first binary search engine performs a predetermined number of iteration in searching a lookup table in stage 1 memory (*a search engine configured to first search said cache or ARL cache table of claim 7*) and the second binary search engine performs binary search on a lookup table in primary memory based on the results from the first binary search engine (*and then search said table or ARL table of claim 7 based on search results of said cache, said search engine connected to said table and said cache, figure 3*).

Re claims 2, 8, and 17, Michels discloses a search engine with a first binary search engine (*a search stage zero segment, figure 3, element 66*) connected to a stage 1 memory (*cache, figure 3, element 70*) and a second binary search engine (*a search stage one segment, figure 3, element 68*) connected to a primary memory (*table, figure 3, element 58*) (*a search engine comprising a search stage zero segment configured to search said cache in said first number of search cycles, said search stage zero segment connected to said cache, and a search stage one segment configured to search said table in a second number of search cycles based on search results of said cache, said search stage one segment connected to said search stage zero segment and said table, column 3, lines 9-16; figure 3; column 5, lines 33-36*).

Re claims 4, 6, 10, 12, 15, 19, and 21, Michels discloses that the first binary search engine performs the first eight iterations of the search and the second binary

search engine performs the last eight iterations (column 6, lines 2-5, *the first number of search cycles used to search the cache is equal to the second number of search cycles used to search the table*).

Claims 3, 5, 9, 11, 14, 18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Michels.

Re claims 3, 5, 9, 11, 14, 18, and 20, Michels discloses all of the limitations of the base claim, but fails to disclose that the first number of search cycles used to search the cache is less than the second number of search cycles used to search the table. Since Michels suggests that the binary search engines can perform any number of iterations depending on the particular application (column 6, lines 22-26), it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the number of iterations to search a lookup table at each search engine so that it will take less time for the binary search engine to search a lookup table with 256 entries than searching a lookup table with 64000 entries.

Claims 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Michels in view of admitted prior art (APA).

Re claims 22-25, Michels discloses all of the limitations of the base claim, but fails to disclose embodiment of the table and search engine on a single substrate. APA discloses implementing various modules, interfaces, and tables onto a single semiconductor substrate (specification, paragraph [0055], lines 1-7). It would have been

obvious to one having ordinary skill in the art at the time the invention was made to modify the configuration of Michels by embedding the table and search engine on a single substrate for the matter of architectural design choice.

(10) Response to Argument

The rejection of claims 1, 2, 4, 6-8, 10, 12, 13, 15-17, 19 and 21 under 35

U.S.C. 102(e)

On pages 8, 9, 11, 12, 15, 16, 18 and 19, applicant argues that Michels does not disclose a table search device comprising the search engine and the table by pointing out that the primary memory of Michels (*the table*, figure 3, element 58) is not part of a search device. The Examiner respectfully disagrees. Michels shows the primary memory as separate and outside of search engine in figure 3, but the Examiner interpreted the primary memory as a part of a search device.

The rejection of claims 3, 5, 9, 11, 14, 18, and 20 under 35 U.S.C. 103(a)

On pages 22-24, applicant argues that Michels does not disclose or suggest that the first number of cycles is less than the second number of search cycles. The Examiner respectfully disagrees. Since Michels suggests that the number of iterations need not be equal depending on the particular application (column 6, lines 22-26), it would have been obvious to one having ordinary skill in the art at the time the invention was made to change the number of iterations to search a lookup table at each search engine.

The rejection of claims 22-25 under 35 U.S.C. 103(a)

On pages 27 and 28, applicant argues that paragraph [0055] on page 16 of the present application indicates that single semiconductor substrate feature is dependent upon the disclosure of the present application, therefore it does not contain any admission of prior. The Examiner respectfully disagrees. The Examiner relied on the concept of implementing the various modules of Michels into a single semiconductor substrate as general knowledge of one of ordinary skill in the art.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Hong Cho

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March 2, 2007

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